ELE 312
Digital Electronics

Textbooks


• Taub and Schilling, *Digital Integrated Electronics*, McGraw-Hill
Contents

• Basic Properties of Digital Integrated Circuits
• Diode Digital Circuits
• BJT Digital Circuits
  – Ebers & Moll equations
  – Transistor modelling
  – State of transistor in a circuit
• Resistor-Transistor Logic (RTL)
• Diode-Transistor Logic (DTL)
• Transistor-Transistor Logic (TTL)
• Schottky Transistor – Transistor Logic (STTL)
• Different TTL Gates
• Emitter-Coupled Logic (ECL)
• MOS Digital Circuits
• NMOS Gates
• CMOS Gates

Properties of Digital Integrated Circuits
Most important elements: Inverter and Noninverter

Inverter Symbols

Noninverter Symbols

Idealized Inverter and Voltage Transfer Characteristics (VTCs)
Propagation Delays

Rise and fall times and turn-on and turn-off times
Power dissipation

Average Power Dissipation = Average Power Supplied

\[ P_{CC} = I_{CC} V_{CC} \]

\[ P_{EE} = I_{EE} V_{EE} \]

Logic Element Equivalent Circuit and Fan-out

driving gate

load gates
Power - Delay Product:

Speed-power product = (Average Power Diss) x (Propagation Delay)

\[ PD = P_{\text{Diss}(\text{avg})} \times t_{\text{P(\text{avg})}} \]
Diodes

Symbols

\[ + V_D - \]
\[ I_D \]
PN Junction

MN Schottky Junction

Shockleys Eq

\[ I_D = I_S \left( e^{V_D/V_T} - 1 \right) \]

for Forward Bias

\[ V_D \cong V_0 = 0.7 \text{ V} \]
IV Characteristics

for PN Junction diodes

for MN Schottky diodes

SPICE model

\[ I_D' = I_s(e^{V_d/N_t} - 1) \]
Basic Logic Gates: AND

Basic Logic Gates: OR
Clamping Diodes

Level shifting diodes

Level Shifting Diode AND Gate

Level Shifting Diode OR Gate
BJT Transistors

BJT Fabrication Example
Multi-Emitter Fabrication Examples

Multi-emitter BJT

Multi-emitter Schottky BJT

NPN BJT

(a)
Ebers-Moll NPN BJT Model

\[
I_E = I_{D, BE} - \alpha R I_{D, BC}
\]
\[
I_C = \alpha_F I_{D, BE} - I_{D, BC}
\]
\[
I_B = I_E - I_C
\]
\[
I_{D, BE} = I_{ES}(e^{\frac{V_{BE}}{V_T}} - 1)
\]
\[
I_{D, BC} = I_{CS}(e^{\frac{V_{BC}}{V_T}} - 1)
\]

Reciprocity theorem
\[
I_S = \frac{I_{ES}}{R} = \frac{I_{CS}}{R}
\]

transport saturation current

BJT Modes of Operation

<table>
<thead>
<tr>
<th>BE junction</th>
<th>BC junction</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reverse</td>
<td>Reverse</td>
<td>Cutoff (OFF)</td>
</tr>
<tr>
<td>Forward</td>
<td>Reverse</td>
<td>Forward active (FA)</td>
</tr>
<tr>
<td>Forward</td>
<td>Forward</td>
<td>Saturation (SAT)</td>
</tr>
<tr>
<td>Reverse</td>
<td>Forward</td>
<td>Reverse active (RA)</td>
</tr>
</tbody>
</table>
Reduced models of the operation modes

(a) Cutoff

\[ I_c = \sigma I_b, \quad \sigma \leq 1 \]

(b) Forward active

\[ I_c = \alpha I_b, \quad \beta < \alpha \]

\[ V_{c(e)}(S&K) = 0.6 \text{ V} \]

(c) Saturation

\[ I_c = \alpha I_b, \quad \beta > \alpha \]

\[ V_{c(e)}(S&K) = 0.8 \text{ V} \]

(d) Reverse active

\[ I_c = \beta I_b, \quad \beta > \alpha \]

\[ V_{c(e)}(R&A) = 0.7 \text{ V} \]

IV Characteristics

- \( \beta_b \gg \beta_n \)
- \( I_c \) increasing
- \( V_{ce}(V) \)
- \( I_c = 6\Delta \)
- \( I_c = 5\Delta \)
- \( I_c = 4\Delta \)
- \( I_c = 3\Delta \)
- \( I_c = 2\Delta \)
- \( I_c = \Delta \)
Modes of Operation

**Cutoff**
- $L_e = 0$
- $V_{e(OFF)} < 0.7 \text{ V}$
- $I_e = 0$

**Forward Active**
- $I_{(FA)} = \beta I_e$
- $V_{e(FA)} = 0.7 \text{ V}$
- $I_e = I_b + I_c$

**Saturation**
- $I_e = I_b + I_c$
- $V_e(SAT) = 0.9 \text{ V}$

**Reverse Active**
- $I_{e(RA)} = \beta I_e$
- $V_e(RA) = 0.7 \text{ V}$
- $I_e = I_b + (-I_c)$

Examples

- $\beta_F = 65$
- $I_C, I_B = ?$
- Base and emitter voltages = ?
TTL Circuit Design

Output-High Pull-up Driver

(a)  

Output-Low Pull-down Driver

Discharge path and Base-Driving circuitry

(a)  

(b)  

(c)
Resistor-Transistor Logic (RTL)
INVERTER

Voltage Transfer Characteristics (VTC)

\[ V_{\text{IL}} = V_{\text{BE(FA)}} \]

\[ V_{\text{IH}} = V_{\text{BE(SAT)}} + \frac{V_{\text{CC}} - V_{\text{CE(SAT)}}}{\beta_f R_C} R_B \]

NAND

NOR
RTL Fan-out

 RTL fan-out analysis

(a)

(b)

(c)
RTL fan-out analysis

Maximum fan-out?

\[ N = \left| \frac{I_{OUT}}{I_{IN}} \right| \]

\[ I_{OUT} = \frac{V_{CC} - V_{OUT}}{R_C} \]

\[ I_{IN} = \frac{V_{OUT} - V_{BE(SAT)}}{R_B} \]

\[ V_{OUT} = V_{IH} \]

\[ V_{IH} = V_{BE(SAT)} + \frac{V_{CC} - V_{CE(SAT)}}{\beta_F R_C} R_B \]
Example 5.2  *Basic RTL Maximum Fan-Out*

What is the maximum fan-out for a basic RTL gate with $V_{CC} = 5 \text{ V}$, $R_S = 10 \text{ k}\Omega$, and $R_C = 1 \text{ k}\Omega$? Let $\beta_F = 25$, $V_{be(SAT)} = 0.8 \text{ V}$, and $V_{ce(SAT)} = 0.2 \text{ V}$.

Example 5.3  *RTL Power Dissipation*

Find the average power dissipated in a basic RTL inverter with

(a) no load

(b) a fan-out of 1

Use $V_{CC} = 5 \text{ V}$, $R_S = 10 \text{ k}\Omega$, and $R_C = 1 \text{ k}\Omega$. Let $\beta_F = 25$, $V_{be(SAT)} = 0.8 \text{ V}$, and $V_{ce(SAT)} = 0.2 \text{ V}$ for the BJTs.
**RTL with Active Pull-up**

<table>
<thead>
<tr>
<th>Element</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{in}$, $R_{de}$</td>
<td>Matched input resistors</td>
</tr>
<tr>
<td>$Q_1$</td>
<td>Drive splitter, pull-down of $Q_2$</td>
</tr>
<tr>
<td>$R_{ec}$</td>
<td>Along with $Q_3$ provides logic inversion to output-high driver</td>
</tr>
<tr>
<td>$R_{em}$</td>
<td>Limits base current to $Q_1$</td>
</tr>
<tr>
<td>$Q_1$</td>
<td>Output inverting BJF output-low driver for current sourcing pull-down</td>
</tr>
<tr>
<td>$Q_2$</td>
<td>Provides active current-sourcing pull-up</td>
</tr>
<tr>
<td>$R_{cp}$</td>
<td>Part of active pull-up</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Element</th>
<th>$V_{OH}$</th>
<th>$V_{OL}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_1$</td>
<td>Cutoff</td>
<td>Saturated</td>
</tr>
<tr>
<td>$Q_2$</td>
<td>Saturated</td>
<td>Cutoff</td>
</tr>
<tr>
<td>$Q_3$</td>
<td>Cutoff</td>
<td>Saturated</td>
</tr>
</tbody>
</table>

**Fan-out of RTL with Active Pull-up**

Determined by the output high state as $Q_3$ is cut-off for low-inputs

<table>
<thead>
<tr>
<th>Element</th>
<th>$V_{oh}$</th>
<th>$V_{ol}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{in}$</td>
<td>$V_{oh}$</td>
<td>$V_{ol}$</td>
</tr>
<tr>
<td>$R_{cp}$</td>
<td>$V_{oh}$</td>
<td>$V_{ol}$</td>
</tr>
<tr>
<td>$Q_3(SAT)$</td>
<td>$V_{oh}$</td>
<td>$V_{ol}$</td>
</tr>
</tbody>
</table>

Simplified output high state  
Simplified input high state
Simplified output-high fan-out configuration

\[
\begin{align*}
I_{\text{OUT}} &= I_{\text{EP}} \cong \frac{V_{\text{CC}} - V_{\text{BE(SAT)}} - V_{\text{OUT}}}{R_{\text{CP}}} \\
V_{\text{OUT(min)}} &= V_{\text{IH}} \\
I_{\text{IN}} &= \frac{V_{\text{OUT}} - V_{\text{BE(SAT)}}}{R_{B} / 2} \\
V_{\text{IH}} &= V_{\text{BE(SAT)}} + \frac{V_{\text{CC}} - V_{\text{BE(SAT)}}}{\beta_{f}R_{C}}R_{B}
\end{align*}
\]

Example 5.5  Maximum Fan-Out of RTL with Active Pull-Up

Compare the maximum fan-out for the RTL inverter with active pull-up (shown in Figure 5.9) with that of basic RTL obtained in Example 5.2. Use the values of \(V_{\text{CC}} = 5\,V\), \(R_{\text{ON}} = R_{\text{OFF}} = 10\,k\Omega\), \(R_{C} = 1\,k\Omega\), \(\beta_{f} = 25\), \(V_{\text{BE(SAT)}} = 0.8\,V\), and \(V_{\text{CE(SAT)}} = 0.2\,V\), which are the same values used in Example 5.2. Also, let \(R_{\text{CP}} = 100\,\Omega\).
Diode-Transistor Logic (DTL)

Basic DTL Inverter

Basic DTL NAND Gate
Diode Modified DTL Inverter

Transistor Modified DTL Inverter

<table>
<thead>
<tr>
<th>Element</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>(D_i)</td>
<td>Input diode, limits (I_B), and provides (\text{ANDing})</td>
</tr>
<tr>
<td>(pR_e)</td>
<td>Limits (I_B)</td>
</tr>
<tr>
<td>((1 - p)R_e)</td>
<td>Self-bias (Q_e)</td>
</tr>
<tr>
<td>(Q_e)</td>
<td>Base-emitter level-shifting for shift of transition width and provides base driving current to (Q_o)</td>
</tr>
<tr>
<td>(D_t)</td>
<td>Level-shifting diode for shift of transition width</td>
</tr>
<tr>
<td>(R_d)</td>
<td>Provides discharge path for saturation stored charge removed from base of (Q_o)</td>
</tr>
<tr>
<td>(Q_o)</td>
<td>Output inverting BJT and output low driver for current sinking pull-down</td>
</tr>
<tr>
<td>(R_e)</td>
<td>Passive current sourcing pull-up</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Element</th>
<th>(V_{OFF})</th>
<th>(V_{OL})</th>
</tr>
</thead>
<tbody>
<tr>
<td>(D_i)</td>
<td>On</td>
<td>Cutoff</td>
</tr>
<tr>
<td>(Q_e)</td>
<td>Cutoff</td>
<td>Forward active</td>
</tr>
<tr>
<td>(D_t)</td>
<td>Cutoff</td>
<td>On</td>
</tr>
<tr>
<td>(Q_o)</td>
<td>Cutoff</td>
<td>Saturated</td>
</tr>
</tbody>
</table>
VTC of Transistor Modified DTL Inverter

\[ V_{OH} = V_{CC} \]
\[ V_{IL} = V_{BE,0(FA)} + V_{BE,L(FA)} \]
\[ V_{OL} = V_{CE,0(SAT)} \]
\[ V_{IH} = V_{BE,0(SAT)} + V_{BE,L(FA)} \]

DTL Fan-out

Determined by the output low state as \( D_1 \) is off for high-inputs
Example: Calculate the DTL fan-out for $\beta_F = 49$ and $\sigma = 0.85$.

Power Dissipation

Example: Calculate the average power dissipation for the above example?
Tansistor-Transistor Logic (TTL)

Basic TTL Inverter

Basic DTL Inverter (compare)

Basic TTL NAND Gate
Actual TTL NAND Gate with Totem Pole Output

<table>
<thead>
<tr>
<th>Element</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q₂</td>
<td>Multi-emitter input BJT, base-collector level shifting of transition width, pull-down of Q₂</td>
</tr>
<tr>
<td>Rₚ</td>
<td>Limits Iₖp</td>
</tr>
<tr>
<td>Q₁</td>
<td>Drive splitter, provides base driving current to Qₚ, base-emitter level shifting for shift of transition width, pull-down of Q₂</td>
</tr>
<tr>
<td>Rₜ</td>
<td>Along with Q₂, provides logic inversion to output-high driver</td>
</tr>
<tr>
<td>Q₀</td>
<td>Output inverting BJT, output low driver for current sourcing pull-down</td>
</tr>
<tr>
<td>D₁</td>
<td>Diode level shifting between VCC and output</td>
</tr>
<tr>
<td>R₀</td>
<td>Provides discharge path for saturation stored charge of Q₀</td>
</tr>
<tr>
<td>Qₚ</td>
<td>Provides active current-sourcing pull-up</td>
</tr>
<tr>
<td>R₂</td>
<td>Part of active pull-up and limits current spikes during output high-to-low transitions</td>
</tr>
<tr>
<td>D₀, D₁</td>
<td>Input clamping diodes to limit the negative swing of the inputs to one diode drop below ground</td>
</tr>
</tbody>
</table>

VTC of an actual TTL Inverter

\[
V_{\text{OH}} = V_{\text{CC}} - V_{\text{BE}p(\text{FA})} - V_{\text{D,L(ON)}}
\]

\[
V_{\text{OL}} = V_{\text{CE,OSAT}}
\]

\[
V_{\text{OH}} = V_{\text{CC}} - I_{\text{RC}} R_{\text{C}} - V_{\text{BE}p(\text{FA})} - V_{\text{D,L(ON)}}
\]

\[
I_{\text{RC}} = I_{\text{B0}} = \frac{V_{\text{BE}p(\text{FA})}}{R_{\text{p}}}
\]

\[
V_{\text{IL}} = V_{\text{BE}p(\text{FA})} - V_{\text{CE}i(\text{SAT})}
\]

\[
V_{\text{IH}} = V_{\text{BE}i(\text{SAT})} + V_{\text{BE}p(\text{SAT})} - V_{\text{CE}i(\text{SAT})}
\]

\[
V_{\text{IB}} = V_{\text{BE}p(\text{FA})} + V_{\text{BE}i(\text{FA})} - V_{\text{CE}i(\text{SAT})}
\]
States of diodes and BJTs

TTL Fan-out

Determined by the output low state as $Q_1$ is cut-off for high-inputs

EOC: Edge of conduction
**Example (TTL Fan-out)**

**Example:** Calculate the TTL fan-out for $\beta_F = 25$, $\sigma = 0.85$ and $\beta_R = 0.1$

\[
I_{RB(OL)} = 675 \mu A \quad I_{IL} = I_{RB(OH)} = 1 \text{ mA} \quad I_{RC(OL)} = 2.5 \text{ mA} \quad I_{OL} = 51.9 \text{ mA}
\]

\[
N = \left| \frac{I_{OL}}{I_{IL}} \right| = 51
\]

**Example (Power Dissipation)**

**Example:** Calculate the average power dissipation for the above example?

\[
P_{CC(avg)} = 10.4 \text{ mW}
\]
Open-Collector TTL

Mostly used in data busses where multiple gate outputs must be ANDed.

- This can be accomplished by using a single pull-up resistor with open-collector TTL gates
- This type of connection is referred to as *wired-AND*.

Low Power TTL (LTTL)

Accomplished simply by increasing the resistance values. However, this results in

- Decreased fan-out
- Longer transient-response times
LTTL Example

Compare the power dissipation of the LTTL and TTL gates.

\[ I_{RB(OL)} = 67.5 \, \mu A \quad I_{RB(OH)} = 100 \, \mu A \quad P_{CC(avg)} = 919 \, \mu W \]
\[ I_{RC(OL)} = 200 \, \mu A \]

TTL vs LTTL power dissipation ratio \( = \frac{10.4}{0.919} = 11.3 \)

High Speed TTL (HTTL)

Accomplished simply by decreasing the resistance values.
However this results in
\[ \text{• Increased power dissipation} \]
Schottky Tansistor-Transistor Logic (STTL)
Multi-Emitter Fabrication Examples

Modes of Operation for SBJT

1. OFF
2. FA
3. On Hard
4. Reverse Schottky
Example (SBJT)

Example: Draw the VTC graph of the SBJT inverter shown below

---

STTL NAND Gate

<table>
<thead>
<tr>
<th>Element</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_1$</td>
<td>Multi-emitter input SBJT, base-collector level-shifting of transition width, pull-down of $Q_1$</td>
</tr>
<tr>
<td>$R_1$</td>
<td>Limits $I_L$</td>
</tr>
<tr>
<td>$Q_2$</td>
<td>Drive splitter, provides base driving current to $Q_{3,4}$, base-emitter level shifting for shift of transition width, pull-down of $Q_1$</td>
</tr>
<tr>
<td>$R_C$</td>
<td>Along with $Q_3$ provides logic inversion to output-high driver</td>
</tr>
<tr>
<td>$Q_{7,8}$</td>
<td>Active Darlington configuration current-sourcing pull-up, base-emitter level-shifting between $V_{CC}$ and output</td>
</tr>
<tr>
<td>$R_{CP}$</td>
<td>Part of active pull-up and limits current spikes during output high-to-low transition</td>
</tr>
<tr>
<td>$R_{DP}$</td>
<td>Provides discharge path for the base of $Q_{3,4}$</td>
</tr>
<tr>
<td>$Q_0$</td>
<td>Active pull-down of $Q_{3,4}$ removes breakpoint between $V_{CC}$ and $V_{dd}$</td>
</tr>
<tr>
<td>$R_{BD}$ &amp; $R_{CD}$</td>
<td>Values ensure that most of $I_C$ is provided as base driving current to $Q_{3,4}$</td>
</tr>
<tr>
<td>$Q_{BD}$</td>
<td>Output inverting BJT, output low driver for current sourcing pull-down</td>
</tr>
<tr>
<td>$D_{C1}$ &amp; $D_{C2}$</td>
<td>Input clamping diodes to limit the negative swing of the inputs to one SSD diode drop below ground</td>
</tr>
</tbody>
</table>
STTL NAND Gate (VTC)

$V_{OH} = V_{CC} - V_{BE1(FA)} - V_{BE2(FA)}$

$V_{OL} = V_{CE}(HARD)$

$V_{IL} = V_{BE0(FA)} + V_{BE2(FA)} + V_{CE2(HARD)}$

$V_{IH} = V_{BE0(HARD)} + V_{BE2(HARD)} - V_{CE2(HARD)}$

STTL NAND Gate (Device states)

<table>
<thead>
<tr>
<th>Transistor</th>
<th>$V_{OH}$</th>
<th>$V_{OL}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_1$</td>
<td>On hard</td>
<td>Reverse</td>
</tr>
<tr>
<td>$Q_2$</td>
<td>Cutoff</td>
<td>On hard</td>
</tr>
<tr>
<td>$Q_3$</td>
<td>Edge of conduction</td>
<td>Forward active</td>
</tr>
<tr>
<td>$Q_4$</td>
<td>Cutoff</td>
<td>Cutoff</td>
</tr>
<tr>
<td>$Q_5$</td>
<td>Cutoff</td>
<td>On hard</td>
</tr>
<tr>
<td>$Q_6$</td>
<td>Cutoff</td>
<td>On hard</td>
</tr>
</tbody>
</table>

Device state table
STTL Fan-out

Determined by the output low state as Q1 is cut-off for high-inputs

Cascaded STTL

\[
N = \frac{I_{\text{ON}}}{I_{\text{I}}}
\]

\[
I_{\text{ON}} = I_{\text{CLO}} = \beta I_{\text{BLO}}(\text{HARD})
\]

\[
I_{\text{LO}} = I_{\text{CLO}} = I_{\text{CLO}}(\text{HARD})
\]

\[
I_{\text{CLO}} = \frac{V_{\text{BE}}}{{R_{\text{CD}}}}
\]

\[
I_{\text{BLO}}(\text{HARD}) = I_{\text{E(S)}}(\text{HARD}) - I_{\text{C,D}}(\text{HARD})
\]

\[
I_{\text{E,S}}(\text{HARD}) = I_{\text{BS}} + I_{\text{CS}}
\]

Path 1

\[
I_{\text{BS}} = \frac{V_{\text{CC}} - V_{\text{BE}}(\text{HARD}) - V_{\text{CE,SH}}(\text{HARD})}{R_{\text{B}}}
\]

Path 2, 3

\[
I_{\text{CS}} = \frac{V_{\text{CC}} - V_{\text{CE,S}}(\text{HARD}) - V_{\text{BE,OX}}(\text{HARD})}{R_{\text{C}}}
\]

\[
I_{\text{BD}} = \frac{V_{\text{CC}} - V_{\text{BE,D}}(\text{HARD})}{R_{\text{D}}}
\]

\[
I_{\text{BS}} = I_{\text{C,(RS)}} = I_{\text{SD}}
\]

\[
I_{\text{SD}} = \frac{V_{\text{CC}} - V_{\text{BE,D}}(\text{HARD}) - V_{\text{BE,OX}}(\text{HARD})}{R_{\text{B}}}
\]
Example (TTL Fan-out)

**Example:** Calculate the STTL maximum fan-out for $\beta_F = 49$.

\[
I_{RB(OL)} = 1.11 \text{ mA} \quad I_{OL} = 197 \text{ mA} \\
I_{RC(OL)} = 4.11 \text{ mA} \quad I_R = I_{RB(OH)} = 1.32 \text{ mA} \\
I_{RCD(OL)} = 1.20 \text{ mA} \\
I_{E(S)(OL)} = 4.22 \text{ mA} \\
I_{R,O(OL)} = 4.02 \text{ mA}
\]

\[
N = \frac{I_{OL}}{I_R} = 149
\]

Example (Power Dissipation)

**Example:** Calculate the average power dissipation for the above example?

\[
I_{E,P(OL)} = 0.182 \text{ mA} \\
I_{E,P(OH)} = 1.3 \text{ mA}
\]

\[
P_{CC(avg)} = 20.05 \text{ mW}
\]

Low Power STTL (LSTTL)

Accomplished by
1. Increasing the resistance value
2. Diode input section
3. Pull-down enhancements
Low Power STTL (LSTTL)

<table>
<thead>
<tr>
<th>Element</th>
<th>Mode</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>D_1 &amp; D_2</td>
<td>On</td>
<td>Cutoff</td>
</tr>
<tr>
<td>Q_1</td>
<td>Cutoff</td>
<td>On hard</td>
</tr>
<tr>
<td>Q_2</td>
<td>Cutoff</td>
<td>On hard</td>
</tr>
<tr>
<td>Q_3</td>
<td>Edge of conduction</td>
<td>Forward active</td>
</tr>
<tr>
<td>Q_4</td>
<td>Cutoff</td>
<td>Cutoff</td>
</tr>
<tr>
<td>D_n</td>
<td>Cutoff</td>
<td>Cutoff</td>
</tr>
</tbody>
</table>

LSTTL Example

Compare the power dissipation of the LSTTL and STTL gates.

\[ I_{RBO(L)} = 170 \, \mu A \quad I_{RBO(H)} = 210 \, \mu A \quad P_{CC(avg)} = 2.11 \, mW \]

\[ I_{RCL(L)} = 463 \, \mu A \]

STTL vs LSTTL power dissipation ratio = 20.05 / 2.11 = 9.5
Advanced Schottky Transistor-Transistor Logic (ASTTL)

Advanced Schottky Transistor Logic

- Advanced Low-Power Schottky TTL (ALSTTL)
- Fairchild Advanced Schottky TTL (FAST)
- Advanced Schottky TTL (ASTTL)
ALSTTL

Element | Purpose |
--- | --- |
Q<sub>in</sub> & Q<sub>out</sub> | BJT emitter-follower configuration reduces I<sub>B</sub> for V<sub>CE</sub> = 200 mV for V<sub>CC</sub> = 5 V |
R<sub>in</sub> | Limits I<sub>B</sub> |
Q<sub>1</sub> | Drive emitter, provides base driving current to Q<sub>2</sub> base-emitter level-shifting for shutoff transition, pull-down of Q<sub>2</sub> and Q<sub>out</sub> |
R<sub>1</sub> | Along with Q<sub>1</sub> provides base-emitter level-shifting for shutoff transition to output-high driver |
Q<sub>2</sub> | Provides base driving current to Q<sub>Q</sub> |
R<sub>2</sub> | Collector resistor for Q<sub>Q</sub> |
D<sub>Q</sub> & D<sub>QW</sub> | Provides discharge path for base of Q<sub>Q</sub> |
Q<sub>Q</sub> & Q<sub>QW</sub> | Active Darlington configuration ensures pull-up base-emitter level-shifting between V<sub>CC</sub> and output |
K<sub>Q</sub> | Part of active pull-up and limits current source-drain output high-to-low transition |

Element | Purpose |
--- | --- |
R<sub>Q</sub> | Glass emitter of Q<sub>Q</sub> a direct path to output and allows charging of load capacitance before Q<sub>Q</sub> is fully on |
D<sub>Q</sub> | Allows Q<sub>Q</sub> and load capacitance to discharge through collector of Q<sub>Q</sub> |
R<sub>Q</sub> & R<sub>QW</sub> | Values are chosen to ensure most of I<sub>Q</sub> is provided as base driving current to Q<sub>Q</sub> |
Q<sub>Q</sub> | Output inverting HBT output-low driver for current-sourcing pull-down |
D<sub>Q</sub> & D<sub>QW</sub> | Input clamping diode to limit the negative swing of the inputs to one step below ground |
D<sub>Q</sub> | Output clamping diode, serves some purpose as D<sub>Q</sub> at the input |

**ALSTTL VTC**

\[ V_{OH} = V_{CC} - V_{BE,0(FA)} \]
\[ V_{OL} = V_{CEO(HARD)} \]
\[ V_{IL} = V_{BE,0(FA)} + V_{EIP,0(FA)} \]
\[ V_{IH} = V_{BE,0(HARD)} + V_{BE,0(HARD)} + V_{BE,SB(HARD)} - V_{BE,0(FA)} \]
ALSTTL VTC

<table>
<thead>
<tr>
<th>Element</th>
<th>$V_{OH}$</th>
<th>$V_{OL}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_{PB}$</td>
<td>On</td>
<td>Cutoff</td>
</tr>
<tr>
<td>$Q_{p}$</td>
<td>Cutoff</td>
<td>On hard</td>
</tr>
<tr>
<td>$Q_{DB}$</td>
<td>Cutoff</td>
<td>On hard</td>
</tr>
<tr>
<td>$D_{p}A$ &amp; $D_{p}B$</td>
<td>Cutoff</td>
<td>Cutoff</td>
</tr>
<tr>
<td>$Q_{p}$</td>
<td>Cutoff</td>
<td>On hard</td>
</tr>
<tr>
<td>$Q_{d}$</td>
<td>Cutoff</td>
<td>On hard</td>
</tr>
<tr>
<td>$Q_{q}$</td>
<td>EOC</td>
<td>Forward active</td>
</tr>
<tr>
<td>$Q_{p}$</td>
<td>Cutoff</td>
<td>Cutoff</td>
</tr>
<tr>
<td>$D_{p}$</td>
<td>Cutoff</td>
<td>Cutoff</td>
</tr>
</tbody>
</table>

FAST

<table>
<thead>
<tr>
<th>Element</th>
<th>Purpose</th>
<th>Element</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>$D_{f}$ &amp; $D_{p}$</td>
<td>Input diode</td>
<td>$D_{p}$</td>
<td>Alters $Q_{d}$ to discharge through collector of $Q_{a}$ and discharges $Q_{d}$ when $Q_{d}$ is forward active</td>
</tr>
<tr>
<td>$R_{b}$</td>
<td>Limits $I_{b}$</td>
<td>$Q_{a}$</td>
<td>Active pull-down of $Q_{a}$ returns</td>
</tr>
<tr>
<td>$Q_{a}$</td>
<td>Pull-up resistor</td>
<td>$R_{b}$ &amp; $R_{c}$</td>
<td>Values are chosen to ensure end of $Q_{a}$ is not driven through $Q_{a}$</td>
</tr>
<tr>
<td>$R_{b}$</td>
<td>Pull-up resistor</td>
<td>$Q_{a}$</td>
<td>Active pull-down of $Q_{a}$</td>
</tr>
<tr>
<td>$R_{c}$</td>
<td>Pull-up resistor</td>
<td>$Q_{a}$</td>
<td>Current from pull-up diode</td>
</tr>
<tr>
<td>$Q_{a}$</td>
<td>Pull-up resistor</td>
<td>$R_{b}$ &amp; $R_{c}$</td>
<td>Active pull-up resistor</td>
</tr>
<tr>
<td>$R_{e}$</td>
<td>Collector resistor</td>
<td>$D_{p}$</td>
<td>Input steering diode to limit the negative going of the inputs to one clade drop</td>
</tr>
<tr>
<td>$D_{p}$</td>
<td>Collector diode</td>
<td>$D_{p}$</td>
<td>Current steering diode, senses same current in $D_{p}$ and $D_{p}$ at the input</td>
</tr>
<tr>
<td>$Q_{p}$</td>
<td>Current steering diode</td>
<td>$D_{p}$</td>
<td>Collector steering diode, senses same current in $D_{p}$ and $D_{p}$ at the input</td>
</tr>
<tr>
<td>$R_{d}$</td>
<td>Pull-up resistor</td>
<td>$D_{p}$</td>
<td>Input steering diode, senses same current in $D_{p}$ and $D_{p}$ at the input</td>
</tr>
<tr>
<td>$R_{p}$</td>
<td>Pull-up resistor</td>
<td>$D_{p}$</td>
<td>Current steering diode, senses same current in $D_{p}$ and $D_{p}$ at the input</td>
</tr>
<tr>
<td>$D_{p}$</td>
<td>Pull-up resistor</td>
<td>$D_{p}$</td>
<td>Input steering diode, senses same current in $D_{p}$ and $D_{p}$ at the input</td>
</tr>
<tr>
<td>$D_{p}$</td>
<td>Pull-up resistor</td>
<td>$D_{p}$</td>
<td>Current steering diode, senses same current in $D_{p}$ and $D_{p}$ at the input</td>
</tr>
</tbody>
</table>
FAST VTC

\[ V_{OH} = V_{CC} - V_{BE,P(FA)} \]
\[ V_{OL} = V_{CE,O(HARD)} \]

\[ V_{IL} = V_{BE,O(FA)} + V_{BE,S(FA)} + V_{BE,SB(FA)} - V_{D,IA(ON)} \]
\[ V_{IH} = V_{BE,O(HARD)} + V_{BE,S(HARD)} + V_{BE,SB(HARD)} - V_{D,IA(ON)} \]

ASTTTL
<table>
<thead>
<tr>
<th>Element</th>
<th>Purpose</th>
<th>Element</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q₁ &amp; Q₂</td>
<td>Input diodes</td>
<td>D₁</td>
<td>Allows Q₂ to discharge through collector of Q₂ and base of Q₂a when Q₂a is forward active</td>
</tr>
<tr>
<td>Q₁a &amp; Q₂a</td>
<td>Input clamping diode</td>
<td>R₁b &amp; R₁c</td>
<td>When all transistors are off, Q₂a is provided as base driving current to Q₂a</td>
</tr>
<tr>
<td>R₁a</td>
<td>Limits I₁a</td>
<td>Q₁b</td>
<td>Output circuit in E, output low driver for current sourcing pull-down</td>
</tr>
<tr>
<td>Q₁ &amp; Q₂a</td>
<td>Drive emitter, provides base driving current to Q₂a, base-emitter level shifting for shift of saturation width, pull-down of Q₁ and Q₂a</td>
<td>D₂a</td>
<td>Input clamping diode to limit the negative voltage of the inputs in one diode drop below ground</td>
</tr>
<tr>
<td>R₂a</td>
<td>Collects emitter for Q₂a</td>
<td>R₂b &amp; R₂c</td>
<td>Output clamping diode, serves same purpose as Q₂a in input</td>
</tr>
<tr>
<td>Q₁b &amp; Q₂b</td>
<td>Provides base driving current to Q₂b</td>
<td>Q₁c</td>
<td>During output low-to-high transition, indicates a current which turns on Q₂b</td>
</tr>
<tr>
<td>Q₁b &amp; Q₂b</td>
<td>Provides discharge path for base of Q₂b</td>
<td>Q₁d</td>
<td>During output low-to-high transition, indicates a current which turns on Q₂b</td>
</tr>
<tr>
<td>Q₁b &amp; Q₂b</td>
<td>Active Designation configuration current-switching pull-up, base-emitter level-shifting between VCC and output</td>
<td>Q₁e</td>
<td>During output high-to-low transition, indicates a current which turns on Q₂b</td>
</tr>
<tr>
<td>Q₁b &amp; Q₂b</td>
<td>Allows discharge path for base of Q₂b</td>
<td>D₁b &amp; D₁c</td>
<td>Along with Q₂b provides a discharge path for Q₂b</td>
</tr>
<tr>
<td>Q₁b &amp; Q₂b</td>
<td>Pulls down base of Q₂b during rapid switching</td>
<td>D₁d &amp; D₁e</td>
<td>Limits pull-down of Q₂b to an adequate level without oscillation</td>
</tr>
<tr>
<td>Q₁b &amp; Q₂b</td>
<td>Provides reference voltage to the base of Q₂b</td>
<td>Q₁f</td>
<td>Decreases rise time at initiation of low-to-high transition</td>
</tr>
<tr>
<td>R₂c</td>
<td>Limits base current of Q₂b</td>
<td>D₁a</td>
<td>Additional pull-down of Q₂b, limits base current to collector of Q₂b</td>
</tr>
<tr>
<td>Q₁a &amp; Q₂a</td>
<td>Provides reference voltage to the base of Q₂b</td>
<td>R₂a</td>
<td>Further limits current to and aids in restoring voltage to base of Q₂a</td>
</tr>
</tbody>
</table>
Other TTL Gates

- AND gates
- NOR gates
- OR gates
- AND-OR-INVERT (AOI) gates
- XOR gates
- Schmitt Trigger Inverters and NAND gates
- Tri-State buffers
Power Dissipation Example

\[ I_{RB(IL)} = 1 \text{ mA} \quad I_{RB(II)} = 675 \mu\text{A} \quad I_{RC(OL)} = 2.5 \text{ mA} \]
\[ I_{CC(LL)} = 2 \text{ mA} \quad I_{CC(III)} = 4.175 \text{ mA} \]
\[ I_{CO(HL)} = 4.175 \text{ mA} \quad I_{CO(II)} = 3.85 \text{ mA} \]
\[ P_{CC(avg)} = 17.75 \text{ mW} \]
Complex Logic TTL Gate Design

1. ANDing of signals
   - Multi-emitter input BJT sections
2. ORing of signals
   - Multiple input sections (Q_I and R_B)
   - Multiple drive splitting BJTs (Q_S)
3. If non-inverting ORing is desired
   - Additional logic inversion circuitry
4. Totem-pole output branch
Example
Design a complex logic TTL gate that $V_{OUT} = V_A V_B + V_C + V_D V_E V_F$
TTL XOR gate

\[ F = A \oplus B = A \odot B \]

Hysteresis and Schmitt Trigger Gates
Hysteresis

Base-Emitter coupled Schmitt Trigger Non-inverting circuit

\[ V_{\text{OHI}} = V_{\text{CC}} \]

\[ V_{\text{CES}} = \frac{V_{\text{CC}} - V_{\text{BE(HA)}}}{R_{\text{CES}}} - \frac{V_{\text{CC}} - V_{\text{CE(SAT)}}}{R_{\text{CES}}} + V_{\text{CE(SAT)}} \]

\[ R_{m} = R_{\text{CSI}} \parallel R_{\text{CIS}} \parallel R_{E} \]

\[ V_{\text{DS}} = \frac{V_{\text{CC}} - V_{\text{BE(HA)}}}{R_{\text{CSI}}} - \frac{V_{\text{CC}} - V_{\text{CE(SAT)}}}{R_{\text{CIS}}} R_{m} + V_{\text{BE(SAT)}} \]

\[ V_{\text{DS}} = \frac{V_{\text{CC}} + \alpha V_{\text{BE(HA)}} - V_{\text{BE(SAT)}}}{\alpha} \]

\[ \alpha = \frac{R_{\text{CSI}}}{R_{E}} + 1 \]
Example

Find the $V_{OHS}$, $V_{OLS}$, $V_{RIS}$ and $V_{IDS}$ points where $R_{CS1} = 4\, \text{k}\Omega$, $R_{CS2} = 2.5\, \text{k}\Omega$, and $R_{ES} = 1\, \text{k}\Omega$.

- $V_{OHS} = 5\, \text{V}$
- $R_{eq} = 606\, \Omega$
- $V_{OLS} = 2\, \text{V}$
- $V_{RIS} = 2.5\, \text{V}$
- $I_{CS1} = 1.05\, \text{mA}$
- $V_{IDS} = 1.66\, \text{V}$
- $I_{CS1} = 1.92\, \text{mA}$

TTL Schmitt Trigger NAND gate
Example

Find the $V_{OH}$, $V_{OL}$, $V_{IH}$ and $V_{ID}$ points where $R_{CS1} = 4\,k\Omega$, $R_{CS2} = 2.5\,k\Omega$, and $R_{ES} = 1k\Omega$.

$V_{CS} = 3.6V$

$V_{ES} = 2.5V$

$V_{II} = 1.8V$

$V_{SS} = 0.96V$

$V_{IE} = 0.2V$

$V_{DS} = 1.66V$

TTL Tri-state Buffers
TTL Tri-state Buffers

Connecting TTL Tri-state buffers to a Bus
Emitter-Coupled Logic (ECL)

Basic ECL Inverter/Non-inverter (ECL Current Switch)
Basic ECL Inverter/Non-inverter VTC

According to inverting output: \( V_{\text{INV}} \)

\[
V_{\text{OH}} = V_{\text{CC}}
\]

\[
V_{\text{OL}} = V_{\text{CC}} - \frac{V_{\text{IH}} - V_{\text{BE(ECL)}} + V_{\text{BE}}}{R_E} R_C
\]

\[
V_s = \frac{V_{\text{CC}} + V_{\text{BC(SAT)}} + \frac{R_C}{R_E} (V_{\text{BE(SAT)}} - V_{\text{BE}})}{1 + \frac{R_C}{R_E}}
\]

Example

Calculate the critical VTC points for the ECL current switch

\( V_{\text{CC}} = 5V, \ V_{\text{EE}} = 0V, \ V_{\text{BB}} = 2.6V, \ R_C = R_{CR} = R_E = 1k\Omega, \)

\( V_{\text{BE(ECL)}} = 0.75V, \ V_{\text{BE(SAT)}} = 0.8V, \ V_{\text{BC(SAT)}} = 0.6V \)

\[
V_{\text{OH}} = 5V \quad V_{\text{IL}} = 2.55V \quad V_s = 3.2V
\]

\[
V_{\text{OL}} = 3.10V \quad V_{\text{IH}} = 2.65V \quad V_{\text{INV}} (V_{\text{IN}} = V_s) = 2.6V
\]
Basic ECL NOR/OR Gate
Example

Find the logical swing, noise margins and noise immunities for the MECL I circuit above.

\[ \beta_F = 49, \ V_{BE(ECL)} = 0.75V, \ V_{BE(FA)} = 0.75V, \ V_{BE(SAT)} = 0.8V, \ V_{BC(SAT)} = 0.6V \]

\[
V_{OH} = -0.76V \]
\[
V_{OL} = -1.55V \]
\[
V_{IL} = -1.225V \]
\[
V_{IH} = -1.125V \]
\[
V_{LS} = 0.79V \]
\[
V_{NMH} = 0.365V \]
\[
V_{NML} = 0.325V \]
\[
V_{NHI} = 0.53V \]
\[
V_{NIL} = 0.475V \]
MECL I Fanout

\[ I_{OH} = I_{E,BN(FA)} - I_{EDN} \]
\[ I_{RDN} = \frac{V_{OH} + V_{EE}}{R_{DN}} \]
\[ I_{E,BN(FA)} = \frac{V_{OH} - V_{BE(ECL)}}{R_{CI}} \]
\[ I_{HI} = \frac{I_{RE}}{\beta_e + 1} \]
\[ I_{IE} = \frac{V_{E} + V_{EE}}{R_{E}} \]
\[ V_{E} = V_{OH} - V_{BE(ECL)} \]

Fan-out Example

Find the maximum fan-out for the MECL I circuit above

\[ \beta_e = 49, V_{BE(ECL)} = 0.75\,V, V_{BE(FA)} = 0.75\,V, V_{BE(SAT)} = 0.8\,V, V_{BC(SAT)} = 0.6\,V \]
Assume load gates reduce \( V_{OH} \) by 0.03 volts.

\[ V_{OH} = -0.79\,V \]
\[ I_{RDN} = 2.205 \,mA \]
\[ I_{E,BN} = 148 \,\mu A \]
\[ I_{E,BN} = 7.4 \,mA \]
\[ I_{OH} = 5.2 \,mA \]
\[ I_{RE} = 2.95 \,mA \]
\[ V_{E} = -1.54 \,V \]
\[ I_{RE} = 59 \,\mu A \]
\[ I_{HI} = \frac{I_{OH}}{I_{IH}} = 87 \]
Power Dissipation Example

Find the average power dissipated in the MECL I circuit above

\[ I_{RE(NOH)} = 2.64 \text{ mA} \]
\[ I_{RDNOH} = 2.22 \text{ mA} \]
\[ I_{RDOH} = 1.825 \text{ mA} \]
\[ I_{REE(NOH)} = 6.685 \text{ mA} \]
\[ P_{EE(\text{avg})} = 35.6 \text{ mW} \]

Other ECL Gates
DeMorgan’s Theorems

- NOR and OR using ANDs and NANDs
  - NOR: \( \overline{A + B} = \overline{A} \cdot \overline{B} \)
  - OR: \( A + B = \overline{\overline{A} \cdot \overline{B}} \)

- NAND and AND using ORs and NORs
  - NAND: \( \overline{A \cdot B} = \overline{A} + \overline{B} \)
  - AND: \( A \cdot B = \overline{\overline{A} + \overline{B}} \)

Example

Implement the following logic using only ECL gates

\((A + B)(\overline{C + D})\)

Solution:

\((A + B)(\overline{C + D}) \equiv (A + B) + (C + D)\)
Complex Logic Gates with Collector Dotting

Any combination of OR-ANDing is possible with the collector dotting design method using the following rules:

1. ORing of signals is performed by multiple input BJT current switches.
2. ANDing of ORed signals is performed by placing multiple current switch input sections in parallel.
3. A single output buffer is taken from the common collector of all current switch reference BJT s.
4. A single bias network similar to that shown in Figure 15.3a is connected to the common base and collector of the reference BJT in all current switch input sections.
Example

Series Gating – Basic ECL NAND/AND Current Switch
Complex Logic Gates with Series Gating

Any combination of OR-AND-Ing along with the complementing OR-AND-Ing inverting can be obtained by obeying the following five steps:

1. OR-ing of signals is performed by parallel input BITs in a single emitter coupled switch.
2. AND-Ing of OR-ed signals is performed by series gating the individual current switches.
3. Output buffers are taken from both collectors of the top current switch.
4. A multiple bias reference circuit is needed for each level of series gating (AND-Ing); the temperature compensating bias network of Figure 15.9a provides two bias voltages: \( V_{BB} \) and \( V_{BP} \).
5. Inputs to emitter coupled switches below the top switch need to be divided down in a manner similar to \( V_{BB} \) through \( D_{LB} R_{LB} \) and \( R_{EB} \) in Figure 15.9a.
Example

ECL XOR/XNOR Gates

V_{cc} > V_{in} > V_{ss}

V_{in} < V_{ss}

Q_{in}, Q_{out}

V_{in}, V_{out}

V_{ss}, V_{cc}

L_{in}, I_{in}

XOR, XNOR

NAND, NOR

11
MOS Logic

- NMOS gates
  - Fabrication
  - Modes of operation
- NMOS Inverters and Analysis
  - General NMOS Inverter
  - Resistor Loaded NMOS Inverter
  - E-MOSFET loaded NMOS Inverter
  - D-MOSFET loaded NMOS Inverter
NMOS (n-channel E-MOSFET) Fabrication Examples

**METAL GATE NMOS**

[Cross-section diagram of a metal gate NMOS]

**SILICON GATE NMOS**

[Cross-section diagram of a silicon gate NMOS]

CMOS Fabrication Example

[Twin-Tub CMOS diagram]
**IV Characteristics**

**SATURATION**

\[ I_d(SAT) = \frac{k}{2} (V_{gs} - V_T)^2 \]

**LINEAR**

\[ I_d(LIN) = k \left[ (V_{gs} - V_T) V_{ds} - \frac{V_{ds}^2}{2} \right] \]

**NMOS modes of operation**

(a) **Cutoff mode**

\[ I_d = 0 \quad V_{in} < V_T \]

(b) **Linear mode**

\[ I_d(LIN) = k \left[ (V_{gs} - V_T) V_{ds} - \frac{V_{ds}^2}{2} \right] \]

(c) **Saturation mode**

\[ I_d(SAT) = \frac{k}{2} (V_{gs} - V_T)^2 \]

(d) **Body-bias effect on threshold voltage**

\[ V_{th} = V_{th0} + \gamma (V_{dd} + 2V_T - V_{dd}) \]

**Process transconductance parameter**

\[ k = \frac{V_T}{I} \]
General NMOS Inverter

Graphical analysis when load is a resistor
Load capacitance

\[ V_{pp} \]
\[ I_L = V_{pp} \]
\[ V_{out} \]
\[ I_{in} \]
\[ V_{in} \]
\[ C_{L} \]

gate output load modelled as a capacitance

Power dissipation

\[ V_{pp} \]
\[ I_L = V_{pp} \]
\[ I_{in} \]
\[ V_{in} \]
\[ C_{L} \]

output load modelled as a capacitance

(a) Static power dissipation

\[ P_{DD} = V_{DD}(I_{DD(OH)} + I_{DD(OL)}) / 2 \]
\[ \approx V_{DD} I_{DD(OL)} / 2 \]

(b) Transient power dissipation

\[ P_{D} = C_{L} f V_{DD}^2 \]

\[ f: \] frequency at which the gate is switched

\[ P_{TOTAL} = P_{DD} + P_{D} \]
Resistor Loaded NMOS

Resistor Loaded NMOS Inverter

![Resistor Loaded NMOS Inverter Diagram]

TABLE 10.1   States of $N_D$ for the Resistor Loaded NMOS Inverter

<table>
<thead>
<tr>
<th>Critical Point</th>
<th>State of $N_D$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>Cutoff</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>Saturation</td>
</tr>
<tr>
<td>$V_{DS}$</td>
<td>Linear</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>Linear</td>
</tr>
<tr>
<td>$V_{DS}$</td>
<td>Saturation</td>
</tr>
</tbody>
</table>

![IV Characteristics Diagram]

![Voltage Transfer Characteristic Diagram]
Propagation Delay

Output load modelled as a capacitance

Fall time

Load capacitance discharging

$\tau_p = \frac{C_{load}}{I_{in}}$

Transfer Delay

$V_{in} = V_{ref}$

$V_{out} = V_{ref}$

MMIC enters saturation mode

MMIC enters linear mode
E-MOSFET Loaded NMOS

E-MOSFET Loaded NMOS Inverter

<table>
<thead>
<tr>
<th>Critical Point</th>
<th>Output $N_0$</th>
<th>Load $N_L$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{om}$</td>
<td>Cutoff</td>
<td>Saturation</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>EOC</td>
<td>Saturation</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Saturation</td>
<td>Saturation</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Linear</td>
<td>Saturation</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Linear</td>
<td>Saturation</td>
</tr>
</tbody>
</table>
D-MOSFET Loaded NMOS

D-MOSFET Loaded NMOS Inverter

<table>
<thead>
<tr>
<th>Critical Point</th>
<th>Output $N_O$</th>
<th>Load $N_L$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OFF}$</td>
<td>Cutoff</td>
<td>Linear</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Saturation</td>
<td>Linear</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Saturation</td>
<td>Saturation</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Linear</td>
<td>Saturation</td>
</tr>
<tr>
<td>$V_{OLR}$</td>
<td>Linear</td>
<td>Saturation</td>
</tr>
</tbody>
</table>
NMOS Gates

Symbol Shorthands

<table>
<thead>
<tr>
<th>Drain or Source</th>
<th>Source or Drain</th>
<th>Drain or Source</th>
<th>Source or Drain</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td></td>
<td>N</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Source or Drain</td>
<td></td>
<td>Source or Drain</td>
</tr>
</tbody>
</table>

Body implied at ground
**NOR Gate**

![NOR Gate Diagram](image)

\[ V_{CL(R \text{ loaded})} = \frac{V_{DD}}{k_0 R_s (V_{DD} - V_{T,DD}) + 1} \]

\[ V_{CL(E-D \text{ loaded})} = \frac{k_2 V_{DD}^2}{2k_0 (V_{DD} - V_{T,DD})} \]

\[ k_0 = k \left( \frac{W_s}{L_s} + \frac{W_s}{L_s} \right) \]

**NOR Gates**

![NOR Gates Diagram](image)

\[ V_{CL(E-D \text{ loaded})} = \frac{k_2 V_{DD}^2}{2k_0 (V_{DD} - V_{T,DD})} \]

\[ V_{CL(\text{two NOR inputs high})} < V_{CL(\text{inverter})} \]
NAND Gate

\[ I_o = I_{on} \]

\[ V_{in} = \begin{cases} 
0 & \text{for } \text{logic 0} \\
1 & \text{for } \text{logic 1} 
\end{cases} \]

\[ V_{out} = \begin{cases} 
0 & \text{for } \text{logic 0} \\
1 & \text{for } \text{logic 1} 
\end{cases} \]

K = \left( \frac{W_{on}}{L_A + L_B} \right)

V_{OL} (NAND) > V_{OL} (Inverter)

OR Gates

\[ F = A + B \]
AND Gates

Example
AOI (AND-OR-INVERT) Gates

Examples
XOR/XNOR Gates

Hysteresis
Schmitt Trigger

Transmission Gate
Transmission Gate Array

CMOS Logic
CMOS Inverter

<table>
<thead>
<tr>
<th>Critical Point</th>
<th>NMOS $N_0$</th>
<th>PMOS $P_0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CM}$</td>
<td>Cutoff</td>
<td>Linear</td>
</tr>
<tr>
<td>$V_{CE}$</td>
<td>S Saturation</td>
<td>Linear</td>
</tr>
<tr>
<td>$V_{CE}$</td>
<td>S Saturation</td>
<td>S Saturation</td>
</tr>
<tr>
<td>$V_{CE}$</td>
<td>Linear</td>
<td>S Saturation</td>
</tr>
<tr>
<td>$V_{CE}$</td>
<td>Linear</td>
<td>Cutoff</td>
</tr>
</tbody>
</table>
Symmetric CMOS Inverter

![Symmetric CMOS Inverter Diagram]

FIGURE 23.5 Symmetric CMOS Inverter with
\[ W_n/L_p = 2.5 \text{ } W_o/L_o \]

Capacitance Effect on Transition - 1

![Capacitance Effect on Transition Diagram]

FIGURE 23.6 CMOS Inverters: Output High to Low
- Transition: full slope input and on fast response curves.
- The load capacitance discharges through active PMOS
- The output voltage sags by an amount: \[ \Delta V = \frac{V_{DD}C_{load}}{R_{load}} \]
Capacitance Effect on Transition - 2

Electrostatic Discharge (ESD) Protection

FIGURE 23.21 Diode Input Protection Circuitry for Silicon-Gate CMOS. (a) Circuitry, (b) Diode is laid out as a base-collector connected BJT diode.
CMOS Gates

Symbol Shorthands
CMOS NAND Gate

- Parallel PMOS pull-up
- Stacked NMOS pull-down

<table>
<thead>
<tr>
<th>$V_A$</th>
<th>$V_B$</th>
<th>$N_A$</th>
<th>$N_B$</th>
<th>$P_A$</th>
<th>$P_B$</th>
<th>Pull-Up Path(s)</th>
<th>Pull-Down Path</th>
<th>$V_{OUT}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>low</td>
<td>low</td>
<td>off</td>
<td>off</td>
<td>on</td>
<td>on</td>
<td>$P_A$, $P_B^*$</td>
<td>none</td>
<td>high</td>
</tr>
<tr>
<td>low</td>
<td>high</td>
<td>off</td>
<td>on</td>
<td>off</td>
<td>on</td>
<td>$P_A$, $P_B$</td>
<td>none</td>
<td>high</td>
</tr>
<tr>
<td>high</td>
<td>low</td>
<td>on</td>
<td>off</td>
<td>off</td>
<td>on</td>
<td>$P_B$</td>
<td>none</td>
<td>high</td>
</tr>
<tr>
<td>high</td>
<td>high</td>
<td>on</td>
<td>on</td>
<td>off</td>
<td>off</td>
<td>none</td>
<td>$N_A$ and $N_B^{**}$</td>
<td>low</td>
</tr>
</tbody>
</table>

*For $V_A$ and $V_B$ low, two output pull-up paths to $V_{DD}$ are present through $P_A$ and $P_B$.

**For $V_A$ and $V_B$ high, a single output pull-down path to ground through $N_A$ and $N_B$ is present.

CMOS NAND Gates

- Parallel PMOS pull-up
- Stacked NMOS pull-down

$$W_P = 2 \times \frac{1}{2} W_N$$

$$W_P = 2 \times \frac{1}{2} W_N$$

CMOS pair A  CMOS pair B  CMOS pair i
CMOS NOR Gate

\[
\frac{W_L}{W_W} = \frac{2I_{DQ}}{I_{DDQ}}
\]

- stacked PMOS pull-up
- parallel NMOS pull-down

<table>
<thead>
<tr>
<th>(V_A)</th>
<th>(V_B)</th>
<th>(N_A)</th>
<th>(N_B)</th>
<th>(P_A)</th>
<th>(P_B)</th>
<th>Pull-Up Path</th>
<th>Pull-Down Path(s)</th>
<th>(V_{OUT})</th>
</tr>
</thead>
<tbody>
<tr>
<td>low</td>
<td>low</td>
<td>off</td>
<td>off</td>
<td>on</td>
<td>on</td>
<td>(P_A) and (P_B)*</td>
<td>none</td>
<td>high</td>
</tr>
<tr>
<td>low</td>
<td>high</td>
<td>off</td>
<td>on</td>
<td>on</td>
<td>off</td>
<td>none</td>
<td>(N_B)</td>
<td>low</td>
</tr>
<tr>
<td>high</td>
<td>low</td>
<td>on</td>
<td>off</td>
<td>on</td>
<td>off</td>
<td>none</td>
<td>(N_A)</td>
<td>low</td>
</tr>
<tr>
<td>high</td>
<td>high</td>
<td>on</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>none</td>
<td>(N_A), (N_B)**</td>
<td>low</td>
</tr>
</tbody>
</table>

*For \(V_A\) and \(V_B\) low, a single output pull-up path to \(V_{DDQ}\) through \(P_A\) and \(P_B\) is present.

**For \(V_A\) and \(V_B\) high, two output pull-down paths to ground are present through \(N_A\) and \(N_B\).

CMOS NOR Gates

\[
\frac{W_L}{W_W} = \frac{I_{DQ}}{I_{DDQ}}
\]

- stacked PMOS pull-up
- parallel NMOS pull-down

CMOS pair A
CMOS pair B
CMOS pair \(i\)
CMOS AND/NAND Gate

CMOS OR/NOR Gate

FIGURE 24.15 Block Diagram Representing Transistor Configuration of Two-input CMOS NOR Gate
CMOS AOI Gates

\[ F = \overline{A \land C \lor B \land D} \]

(a)
CMOS AND-OR Gate

(a) 

CMOS OAI Gates

(b) 

F = AC + BD

F = AC + BD
CMOS AOI Gates

Example
XOR Gate